CLAIMS

What is claimed is:

1. An integrated circuit package comprising:

a first substrate having a first surface and a second surface, the first substrate including at least one heat-generating circuit and having a first coefficient of thermal expansion; and

a second substrate having at least a first surface and a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second substrate being thermally coupled to the second surface of the first substrate, the second substrate functioning to thermally conduct heat generated by the at least one heat-generating circuit away from the at least one heat-generating circuit.

2. The integrated circuit package of claim 1, wherein the second substrate has a second surface, the integrated circuit package further comprising:

a metallic heat sink thermally coupled to the second surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

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3. The integrated circuit package of claim 1, wherein the coupling between the metallic heat sink and the second substrate is such as to accommodate movement of the metallic heat sink with respect to the second substrate.

4. The integrated circuit package of claim 2, wherein the coefficient of thermal expansion of the metallic heat sink is approximately seven times greater than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

5. The integrated circuit package of claim 1, further comprising:

an adhesive layer having a first surface and a second surface, the first surface of the adhesive layer being physically connected to the second surface of the first substrate, the second surface of the adhesive layer being physically connected to the first surface of the second substrate, wherein a thickness of the adhesive layer is less than or equal to approximately one-sixth of a thickness of the first substrate and wherein the adhesive layer functions to thermally couple the first substrate to the second substrate and to position the second substrate in a fixed relation with respect to the first substrate.

6. The integrated circuit package of claim 1, further comprising:

a printed circuit board substrate having at least a first surface, the printed circuit board substrate including at least one conductive trace;

an adhesive layer having a first surface and a second surface, the first surface of the adhesive layer being physically connected to the first surface of the printed circuit board substrate, the second surface of the adhesive layer being physically connected to the first surface of the first substrate, wherein the adhesive layer functions to at least

position the first substrate in a fixed relation with respect to the printed circuit board substrate; and

at least one electrically conductive path connecting the at least one heat-generating circuit to the at least one conductive trace.

7. The integrated circuit package of claim 6, wherein the adhesive layer comprises a conductive epoxy.

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8. The integrated circuit package of claim 6, wherein the at least one electrically conductive path comprises at least one wire bond.

9. The integrated circuit package of claim 1, wherein a thickness of the second substrate is greater than a thickness of the first substrate.

10. The integrated circuit package of claim 1, wherein the second substrate includes a second surface, the integrated circuit package further comprising:

a third substrate having a first surface and a second surface, the third substrate including at least one heat-generating circuit and having a third coefficient of thermal expansion;

a fourth substrate having a first surface and a second surface, the fourth substrate having a fourth coefficient of thermal expansion that is substantially equal to the third coefficient of thermal expansion, the first surface of the fourth substrate being thermally coupled to the second surface of the third substrate, the fourth substrate functioning to thermally conduct heat generated by the at least one heat-generating circuit of the third substrate away from the third substrate; and

a metallic heat sink thermally coupled to the second surface of the second substrate and to the second surface of the fourth substrate.

11. The integrated circuit package of claim 10, further comprising:

a printed circuit board substrate that includes a plurality of conductive traces; and

a plurality of electrically conductive paths connecting the at least one heat-generating circuit of the first substrate and the at least one heat-generating circuit of the third substrate to the plurality of conductive traces of the printed circuit board substrate.

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12. The integrated circuit package of claim 1, wherein the first substrate comprises a first semiconductor material and wherein the second substrate comprises one of the first semiconductor material and a second semiconductor material.

13. The integrated circuit package of claim 12, wherein both the first substrate and the second substrate comprise silicon.

14. The integrated circuit package of claim 12, wherein both the first substrate and the second substrate comprise gallium arsenide.

15. The integrated circuit package of claim 12, wherein both the first substrate and the second substrate comprise silicon germanium.

16. The integrated circuit package of claim 1, wherein the first substrate is fabricated from a first organic compound material and wherein the second substrate is fabricated from one of the first organic compound material and a second organic compound material.

17. An integrated circuit package comprising:

a first substrate having a first surface and a second surface, the first substrate including at least one heat-generating circuit and having a first coefficient of thermal expansion;

a second substrate having a first surface and a second surface, the second substrate having a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second substrate being thermally coupled to the second surface of the first substrate, the second substrate functioning to thermally conduct heat generated by the at least one heat-generating circuit away from the at least one heat-generating circuit;

a printed circuit board substrate having at least a first surface, the printed circuit board substrate including at least one conductive trace;

a first adhesive layer having a first surface and a second surface, the first surface of the first adhesive layer being physically connected to the second surface of the first substrate, the second surface of the first adhesive layer being physically connected to the first surface of the second substrate, wherein a thickness of the first adhesive layer is less than or equal to approximately one-sixth of a thickness of the first substrate and wherein the first adhesive layer functions to thermally couple the first substrate to the second substrate and to position the second substrate in a fixed relation with respect to the first substrate;

a second adhesive layer having a first surface and a second surface, the first surface of the second adhesive layer being physically connected to the first surface of the printed circuit board substrate, the second surface of the second adhesive layer being physically connected to the first surface of the first substrate, wherein the second adhesive layer functions to at least position the first substrate in a fixed relation with respect to the printed circuit board substrate;

at least one electrically conductive path connecting the at least one heat-generating circuit to the at least one conductive trace; and

a metallic heat sink thermally coupled to the second surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is

substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

18. A printed circuit board arrangement comprising:

a first integrated circuit comprising:

a first semiconductor substrate having a first surface and a second surface, the first semiconductor substrate including at least a first heat-generating circuit and having a first coefficient of thermal expansion;

a second semiconductor substrate having a first surface and a second surface, the second semiconductor substrate having a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion, the first surface of the second semiconductor substrate being thermally coupled to the second surface of the first semiconductor substrate, the second semiconductor substrate functioning to thermally conduct heat generated by the at least a first heat-generating circuit away from the at least a first heat-generating circuit;

a first printed circuit board substrate having a first surface and a second surface, the first printed circuit board substrate including at least one conductive trace, the second surface of the first printed circuit board including at least one electrically conductive receptacle area;

a first adhesive layer having a first surface and a second surface, the first surface of the first adhesive layer being physically connected to the first surface of the first printed circuit board substrate, the second surface of the first adhesive layer being physically connected to the first surface of the first semiconductor substrate, wherein the first adhesive layer functions to at least position the first semiconductor substrate in a fixed relation with respect to the first printed circuit board substrate;

at least one electrically conductive path connecting the at least a first heat-generating circuit to the at least one conductive trace of the first printed circuit board substrate;

at least a second integrated circuit comprising:

a third semiconductor substrate having a first surface and a second surface, the third semiconductor substrate including at least a second heat-generating circuit and having a third coefficient of thermal expansion;

a fourth semiconductor substrate having a first surface and a second surface, the fourth semiconductor substrate having a fourth coefficient of thermal expansion that is substantially equal to the third coefficient of thermal expansion, the first surface of the fourth semiconductor substrate being thermally coupled to the second surface of the third semiconductor substrate, the fourth semiconductor substrate functioning to thermally conduct heat generated by the at least a second heat-generating circuit away from the at least a second heat-generating circuit;

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a second printed circuit board substrate having a first surface and a second surface, the second printed circuit board substrate including at least one conductive trace, the second surface of the second printed circuit board including at least one electrically conductive receptacle area;

a second adhesive layer having a first surface and a second surface, the first surface of the second adhesive layer being physically connected to the first surface of the second printed circuit board substrate, the second surface of the second adhesive layer being physically connected to the first surface of the third semiconductor substrate, wherein the second adhesive layer functions to at least position the third semiconductor substrate in a fixed relation with respect to the second printed circuit board substrate;

at least one electrically conductive path connecting the at least a second heat-generating circuit to the at least one conductive trace of the second printed circuit board substrate;

a metallic heat sink thermally coupled to the second surface of the second semiconductor substrate and to the second surface of the fourth semiconductor substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion, the second coefficient of thermal

expansion, the third coefficient of thermal expansion and the fourth coefficient of thermal expansion;

a third printed circuit board substrate having a first surface and a second surface, the first surface of the third printed circuit board substrate including a plurality of electrically conductive receptacle areas;

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a first electrically conductive layer physically and electrically connecting the at least one electrically conductive receptacle area of the second surface of the first printed circuit board to at least a first electrically conductive receptacle area of the plurality of electrically conductive receptacle areas of the first surface of the third printed circuit board; and

a second solder layer physically and electrically connecting the at least one electrically conductive receptacle area of the second surface of the second printed circuit board to at least a second electrically conductive receptacle area of the plurality of electrically conductive receptacle areas of the first surface of the third printed circuit board.

19. The printed circuit board arrangement of claim 18, wherein the at least one electrically conductive path of the first integrated circuit comprises only solder and wherein the at least one electrically conductive path of the second integrated circuit comprises only solder.

20. The printed circuit board arrangement of claim 18, wherein the at least one electrically conductive path of the first integrated circuit comprises at least one wire bond and wherein the at least one electrically conductive path of the second integrated circuit comprises at least one wire bond.

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21. A method for fabricating an integrated circuit, the method comprising the steps of:

providing a first substrate, the first substrate including at least one heat-generating circuit and having a first coefficient of thermal expansion;

providing a second substrate, the second substrate having a second coefficient of thermal expansion that is substantially equal to the first coefficient of thermal expansion;

thermally coupling the first substrate to the second substrate, such that, during operation of the integrated circuit, the second substrate thermally conducts heat generated by the at least one heat-generating circuit away from the at least one heat-generating circuit.

22. The method of claim 21 further comprising the steps of:

thermally coupling a metallic heat sink to a surface of the second substrate, wherein a coefficient of thermal expansion of the metallic heat sink is substantially different than the first coefficient of thermal expansion and the second coefficient of thermal expansion.

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23. The method of claim 21, wherein the step of thermally coupling the first substrate to the second substrate comprises the step of attaching the first substrate to the second substrate using an adhesive, wherein a thickness of the adhesive is less than or equal to approximately one-sixth of a thickness of the first substrate.

24. The method of claim 23, wherein the first substrate comprises a first semiconductor substrate, wherein the second substrate comprises a second semiconductor substrate, and wherein the step of attaching is performed using a die attachment technique.

25. The method of claim 21, further comprising the steps of:

attaching the first substrate to a printed circuit board substrate, the printed circuit board substrate including at least one conductive trace; and

electrically connecting the at least one heat-generating circuit to the at least one conductive trace.

26. The method of claim 21, wherein the first substrate comprises a first semiconductor substrate and wherein the step of providing a first substrate comprises the steps of:

fabricating a semiconductor wafer that includes a plurality of semiconductor substrates, each of the plurality of semiconductor substrates including at least one heat-generating circuit; and

separating the first semiconductor substrate from the semiconductor wafer.

27. The method of claim 21, wherein the second substrate comprises a second semiconductor substrate and wherein the step of providing a second substrate comprises the steps of:

fabricating a semiconductor wafer that includes a plurality of blank semiconductor substrates, none of the plurality of blank semiconductor substrates including any heat-generating circuits; and

separating the second semiconductor substrate from the semiconductor wafer.